A CMOS-based Neural Implantable Optrode for Optogenetic Stimulation and Electrical Recording

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***Abstract*—This paper presents a novel integrated optrode for simultaneous optical stimulation and electrical recording for closed-loop optogenetic neuro-prosthetic applications. The design has been implemented in a commercially available 0.35µm CMOS process. The system includes circuits for controlling the optical stimulations; recording local field potentials (LFPs); and onboard diagnostics. The neural interface has two clusters of stimulation and recording sites. Each stimulation site has a bonding point for connecting a micro light emitting diode (µLED) to deliver light to the targeted area of brain tissue. Each recording site is designed to be post-processed with electrode materials to provide monitoring of neural activity. On-chip diagnostic sensing has been included to provide real-time diagnostics for post-implantation and during normal operation.**

I. INTRODUCTION

Optogenetics holds great potential to create the next generation of neuroprosthetic devices. The technique uses gene therapy to photosensitize neuron cells by expressing light sensitive ion channels and pumps on the cell surface. However, such molecules require high intensity irradiance to be activated. Thus, there is a requirement for complementary optoelectronics to complete the prosthesis. Such combined gene-therapy and optoelectronics approach to prosthetics could have applications in artificial vision, auditory systems and brain pacemakers [1-6]. Previously, we developed CMOS driven µLED arrays for retinal prosthesis [2, 5, 7-9], and our interests in this work are utilizing our technology to develop brain implants. The key requirements include an ultra-miniature footprint, low power consumption, biocompatibility and stability.

Last year, we adapted our technology into a CMOS optrode to which µLEDs could be bonded on [10]. The incorporated circuits were capable of controlling optical emission, but not electronic recording. In this paper, we present an advanced design, which can record electrical activity and control the optical stimulus.

While the targeted neurons are activated by light, it is useful to simultaneously observe the neural activity adjacent to the stimulation site, achieving closed-loop neuroprosthesis. To achieve this, rather than recording individual action potentials (APs), we have decided to tune our electronics to local field potentials (LFPs) of neuron activity. There is some evidence in the literature that recording LFPs are more stable than APs for chronic recordings [11, 12], and potentially require less complex post-processing [12].

We have therefore adapted LFP recording circuits from our previous work [13, 14], connecting to a total of four microelectrode sites. Thus, this integrated optrode would be applied for closed-loop neural stimulation and neural recording. Fig. 1(a) shows how this optrode concept will be incorporated with a processing unit as part of an implanted neuroprosthesis.

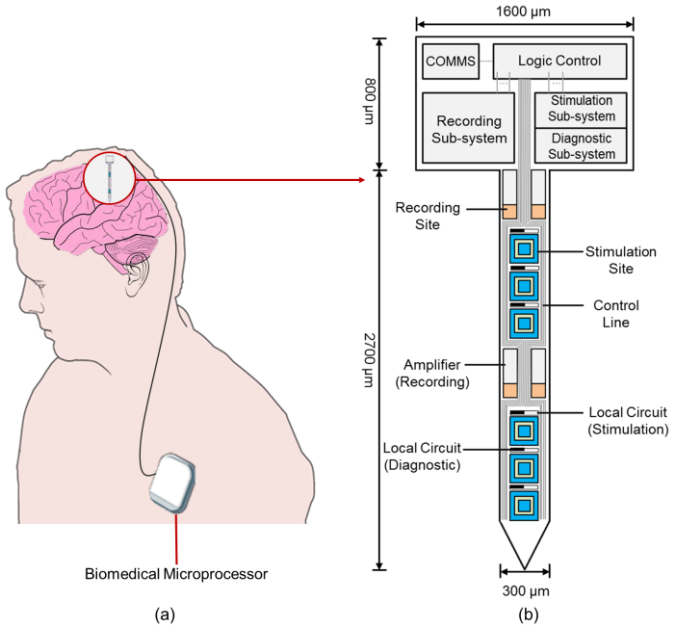

Fig. 1. (a) Proposed Implantable optrode. The optrode will communicate with a biomedical microprocessor for close-loop processing. (b) Basic optrode floorplan illustrating the organisation of the different sub-systems.

We have also updated our optical control, incorporating intensity modulation alongside pulse width modulation (PWM). This is achieved through adjustment of current bias to the LED control by an 8-bit digital-to-analogue converter (DAC), thus achieving a finer overall modulation of intensity. As the optrode (including LEDs) will be implanted into brain tissue, for continuous, long-term operation, the circuit reliability needs to be carefully considered. A risk is that breakage occurs during implantation. To manage this, we have additionally designed and included diagnostic sensing circuitry within the optrode to monitor the mechanical integrity of the substrate.

This paper is organized as follows: Section I introduces the work; Section II details the system architecture; System III describes the circuit implementation; Section IV presents the simulated/measured results and Section V concludes the paper.

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II. System Architecture

The system architecture is shown in Fig.1 (b). This consists of four main sub-systems: optical stimulation, LFP recording, diagnostic sensing and logic control. Along the optrode shaft, there are two clusters of stimulation and recording sites. Each cluster has three optical stimulation sites, and two electrical recording sites. Clustering allows for fine positioning and redundancy. The current optrode is 3.5 mm long whereas the eventual intended dimension will be 6 mm length. This will allow us to include additional stimulation and recording clusters to target specific cell layers in the cortex.

Optical control is via both intensity control electronics and pulse width modulation. The electronic recording system is designed to record LFPs (as opposed to extracellular APs). We have also incorporated diagnostic sensing electronics to determine the operational functionality of the optrode. Diagnostics would detect if there was a shaft break upon brain insertion and determine the stability and any long-term degradation of the optical emitters. Finally, we incorporated a full logic controller which provides a basic command interpreter via a serial peripheral interface (SPI), and a finite state machine (FSM) to address/control each section and for off-chip communication.

III. Circuit Implementation

A. Optical Stimulation Circuit

The optical stimulation circuit is shown in Fig. 2. This consists of three parts: intensity modulation circuitry, memory units (for pulse width modulation) and drive circuitry. A common 8-bit DAC and a transconductance amplifier (TCA) are used to set a control voltage for individual current sources at each LED control site. These are designed on 3 V circuitry converting 0-3 V into 0-1 mA. The control electronics are then formed into an H-bridge configuration. This allows for both light emission and diagnostics setting. The three modes, off, stimulation, diagnostic, are controlled by memory units which can be switched at speed to provide pulse width modulation. A further advantage of the H-bridge is this configuration can additionally be used to characterize the electrical characteristics of the reverse biased LED for future investigation.

It can be seen that the FSM sends commands to local digital control cells and the commands are decoded into four H-bridge control signals, S_{P1}, S_{P2}, S_{N1}, and S_{N2}. These signals are saved by memory cells and then transmitted to H-bridge. Giving different values (0 or 1) to these four control signals, the H-bridge can be configured to achieve four different functions, forward stimulation, reverse stimulation, forward diagnostic and reverse diagnostic. A detailed truth table of this 4-function H-bridge is displayed in Table I.

TABLE I. Truth Table of H-bridge Control Signals

Control Signals				Function
S_{P1}	S_{P2}	S_{N1}	S_{N2}	
0	1	0	1	Forward Stimulation
1	0	1	0	Reverse Stimulation
1	1	0	1	Forward Diagnostic
1	1	1	0	Reverse Diagnostic

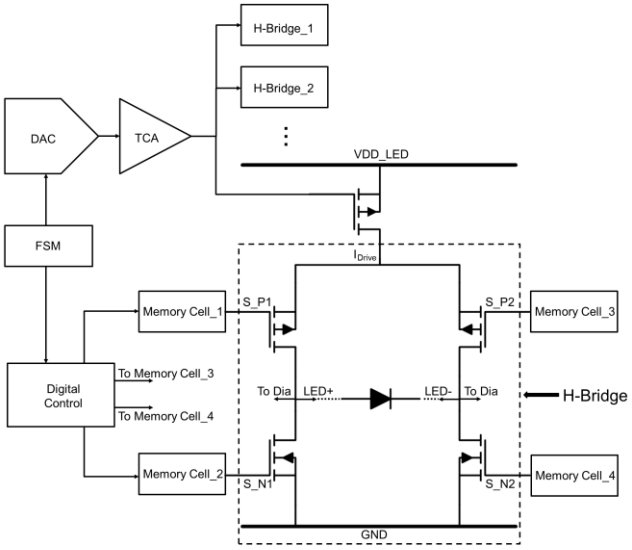

Fig. 2. Schematic diagram of the optical stimulation circuit. I_{Drive} is the LED drive current generated by the DAC and TCA and it is used for LED emission. In the H-bridge block, the LED anode and cathode are also connected to the diagnostic sensing circuit.

B. Diagnostic Sensing Circuit

As the optrode is to be implanted, it is necessary to detect any breakages, particularly at the stimulation sites, to avoid any current discharging into brain tissue. During normal operation, the LED exhibits a diode-like behavior of the current profile through the LED from a fixed power supply. However, if there is some damage to the optrode, e.g. mechanical fracture or contact corrosion between the LED and CMOS circuit, the behavior will differ significantly. This can be easily detected by scanning current through each LED and characterizing their I-V profiles. For contact corrosion, it is expected there will be a large LED series resistance and thus the diode behavior will be more linear. If there is a substrate fracture, an open circuit will be detected. In order to detect these two conditions, we implemented the diagnostic sensing circuit as shown in Fig. 3. In this circuit, a DAC is chosen to set different input voltages to achieve the current scanning via a TCA, and drive the LED. As it is not desired to turn on the LED, we limit the current output range of the diagnostic sensing circuit to 0-10 µA.

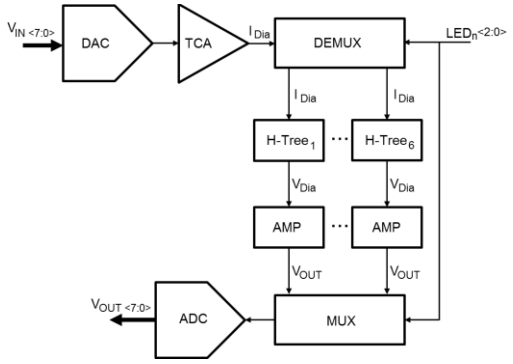

Fig. 3. Block diagram of the diagnostic sensing circuit. Input voltages are generated using a DAC and converted to a "weak" current I_{Dia} by the TCA. I_{Dia} is then fed through an analog demux to drive a specific LED (selected by LED address, LED_n). Voltage across that LED (V_{Dia}) could then be extracted and amplified by a simple amplifier (AMP). At last this amplified output voltage is transmitted to an analogue-to-digital converter (ADC) via an analogue mux.

C. LFP Recording Circuit

The electrical recording sub-system is required to observe the LFP activity at all sites continually. Typically, LFP signals can have amplitudes up to 5-10 mV, with a power spectrum predominantly below 100 Hz. The circuit schematic for the LFP recording subsystem is shown in Fig. 4. This includes four recording channels, a shared successive approximation (SAR) ADC and corresponding control logic. In each recording channel there is a front-end amplifier (FEA) and a 2nd gain stage, which amplifies the input signal to occupy the full dynamic range of the ADC. Here, a capacitive-coupled low noise amplifier (LNA) topology is implemented to minimize the voltage offset of the electrode and provide high input impedance [15]. An analogue multiplexer and a voltage buffer are used to select the output from four channels and feed into ADC.

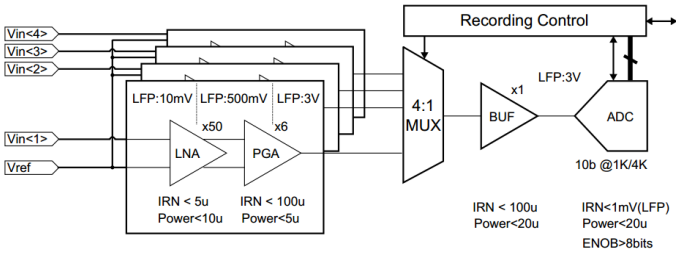

Fig. 4. Circuit schematic of the LFP recording subsystem. FEA is utilized to couple to electrode and provide low-noise amplification. A 2nd stage programmable gain amplifier (PGA) provides further amplification. The amplified signals are then multiplexed, buffered and sampled by the ADC.

D. Logic Control

A basic command interpreter with SPI-based off-chip communication has been included to receive and execute commands. This has been implemented using a FSM, optimized for minimal latency. This receives SPI data (commands) from a master, generates and sends control signals to the different sub-blocks, and transmits data upon request. All operations in the optrode are synchronized to a master clock, except for the SPI transceiver, which uses the SPI clock MCLK. An external global reset is used to reset all internal states.

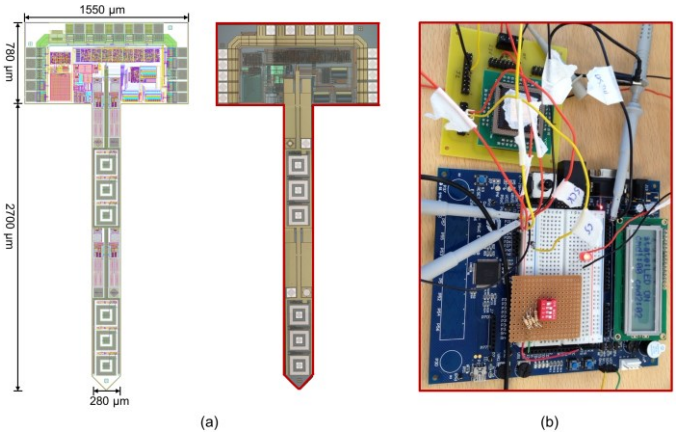

Fig. 5. (a) Optrode layout design and microphotograph. The die area is 1.96mm^2, including the seal ring that has been reserved for protection during post-processing. (b) A photograph of on-bench testing environment.

E. Optrode Fabrication & Post-Processing

The optrode has been fabricated in a standard CMOS process provided by AMS (0.35µm, 2-poly, 4-metal). The chip layout and microphotograph are shown in Fig. 5. The perimeter of the optrode has been sealed using scribe components to prevent leakage into the active devices and/or electrical connection. Furthermore, the top metal layer (Metal 4) has been connected to global ground as a cover to achieve further protection.

Post fabrication, the following processes will be performed: (1) deposition of active electrodes at the recording sites; (2) flip-chip bonding the micro-LEDs; (3) back-grinding to thin wafer; (4) "cutting out" the desired optrode geometry (T-shape) from the CMOS Si die using deep reactive ion etching (DRIE); (5) passivation; (6) connecting the ribbon cable; and (7) encapsulation.

IV. Results

Firstly, we simulated and checked the functionality of optical stimulation circuit. During stimulation, given voltage is generated by the DAC and then converted into the corresponding drive current to bias the LED. In this simulation, a scanning of LED current (I_{LED}) from 0 mA to 1.0 mA is conducted by adjusting DAC value. Then the voltage across LED (V_{LED}) is recorded, and the I-V curve of LED is observed correspondingly, LED luminous intensity is also deduced. Fig.6 illustrates the relationship between the LED voltage/luminous intensity and the drive current.

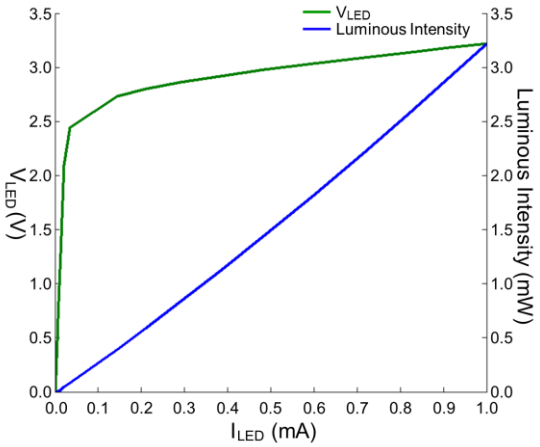

Fig. 6. Correlations of V_{LED} versus I_{LED} and luminous intensity versus I_{LED}.

The functionality of the diagnostic sensing circuit has also been checked through simulations. When the optrode is working under different conditions (i.e. normal condition, optrode rupture and contact corrosion between LED and CMOS), the voltage profile of LED will be varied, and it can be characterized by diagnostic sensing circuit. Fig. 7 shows that sweeping the DAC input voltage (V_{IN}), voltage characteristics of LED under various statuses are obviously different. When the LED is working under normal condition, the range of LED voltage is 0-1.1 V; if a rupture occurs in the optrode, the entire 5 V power supply is observed across the LED; in the event of contact corrosion, the LED voltage increases up to 5 V. Thus, only if we set a scanning of V_{IN}, especially in the range of 2.0-

3.3 V, then any rupture point or contact corrosion can be noticed by diagnostic sensing circuit.

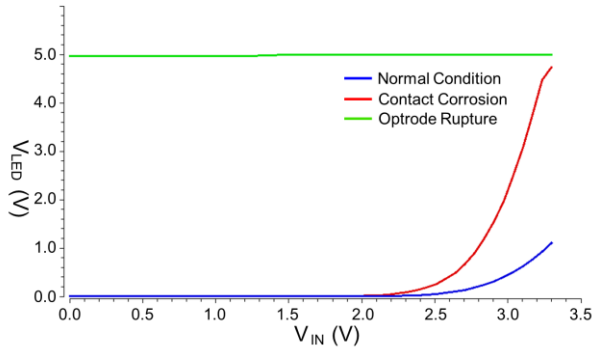

Fig. 7. Voltage profiles of diagnostic sensing circuit under different LED operation scenarios.

Moreover, simulated frequency response for the Gain and Power Supply Rejection Ratio (PSRR) for the LFP recording circuit is shown in Fig 8. The gain response exhibits a band pass characteristic with a high pass corner at 8 mHz, a low pass corner at 9 kHz, and signal gain of 50 dB through 1-300 Hz, where 90 dB PSRR can be found within the required signal band 1-200 Hz. This analogue system provides sufficient gain for the neural signal with minimized supply-induced distortion, and utilizes the full dynamic range of the ADC.

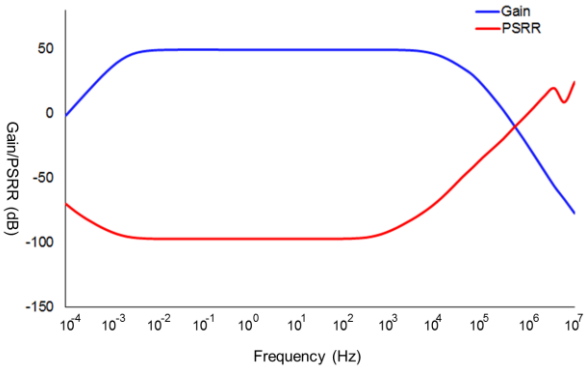

Fig. 8. LFP recording frequency response showing Gain and PSRR.

TABLE II. DESIGN SPECIFICATIONS

System Overview		
	This work	[10]
Technology	AMS 0.35-µm, 2P4M CMOS	X-Fab 0.35-µm, 2P4M CMOS
No. stim. sites, No. rec. sites	6, 4	6, N/A
Optical Stimulation		
LED current range	0 - 1.0 mA	0 - 12.0 mA
Stimulation mode	Bi-direction	Single direction
Modultion methods	PWM, intensity control	PWM only
Diagnostic Sensing		
In current/Out voltage	0 - 10 µA/ 0 - 5.0 V	0 - 40 µA/ 0 - 5.0 V
LFP Recording		
Gain, PSRR	50 dB, 90 dB	N/A
ADC resolution, sampling rate	10-bit, 500 Hz	N/A

V. CONCLUSION

We have reported a novel CMOS-based optrode design for achieving concurrent multichannel optical stimulation and electrical recording. A summary of design specifications is presented in Table II. Inbuilt diagnostic sensing circuits have been implemented to highly improve system safety and reliability. Detailed simulation results have demonstrated circuit operations. The optrode is currently undergoing extensive electrical characterization and will then be verified experimentally, *in-vivo*.

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